

FIG.1A

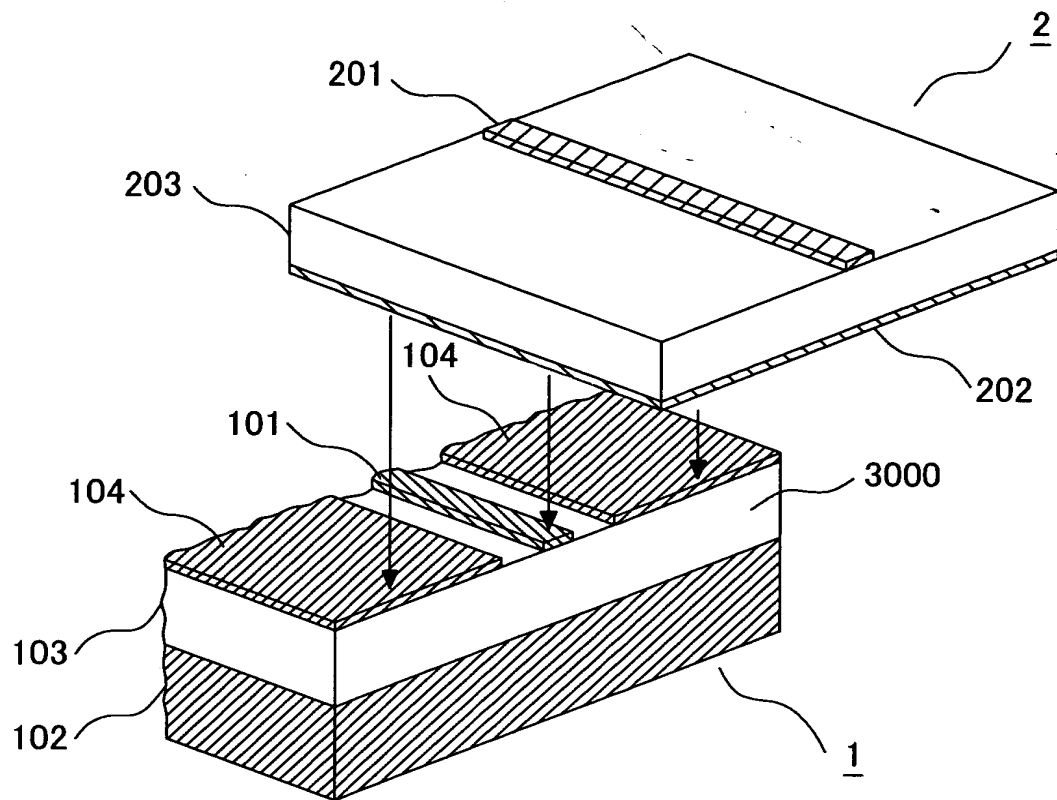


FIG.1B

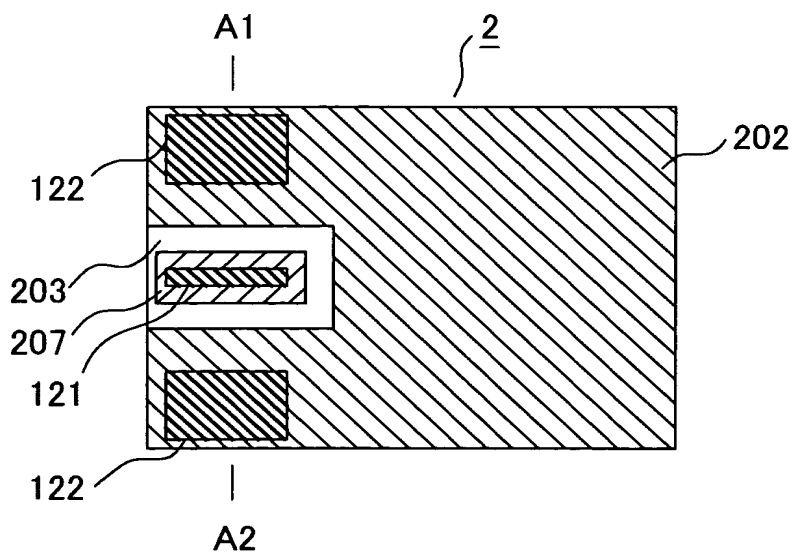


FIG.1C

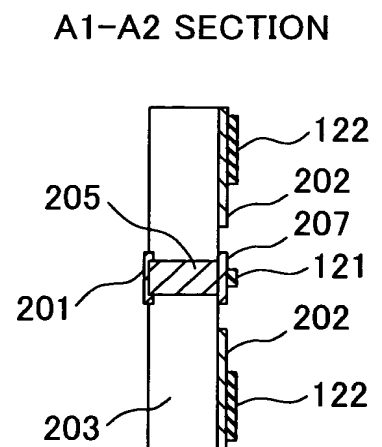


FIG.2A

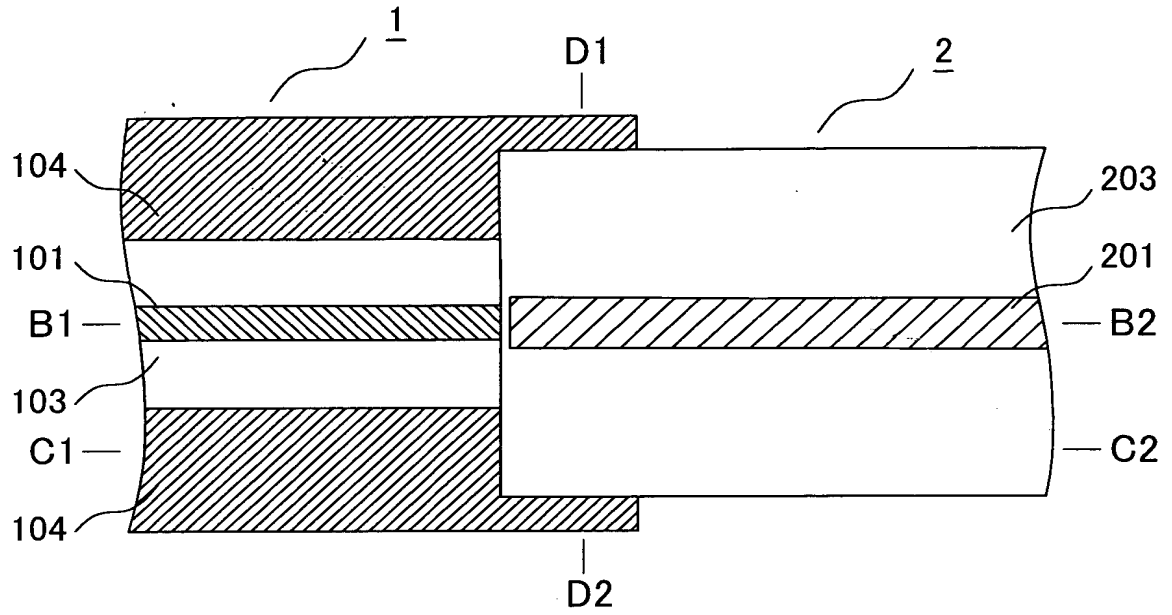


FIG.2B

B1-B2 SECTION

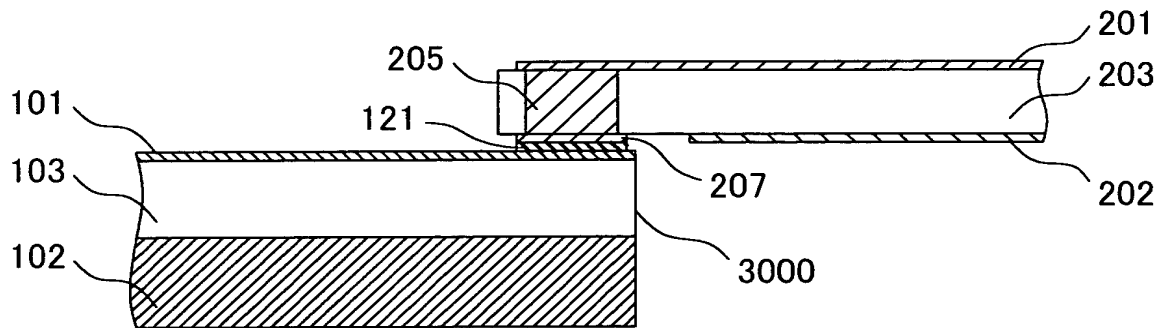


FIG.2C

C1-C2 SECTION

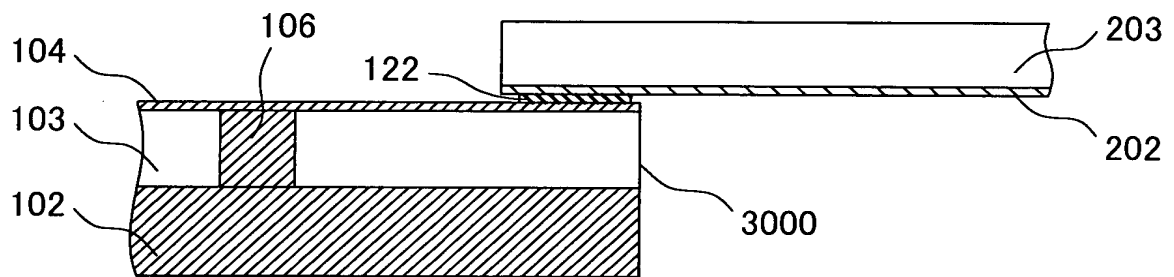


FIG.2D

D1-D2 SECTION

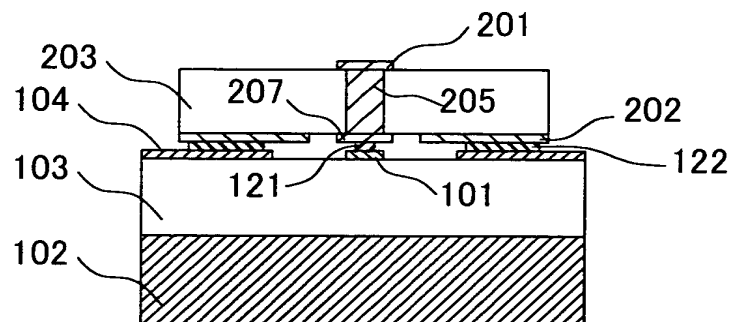


FIG.3A

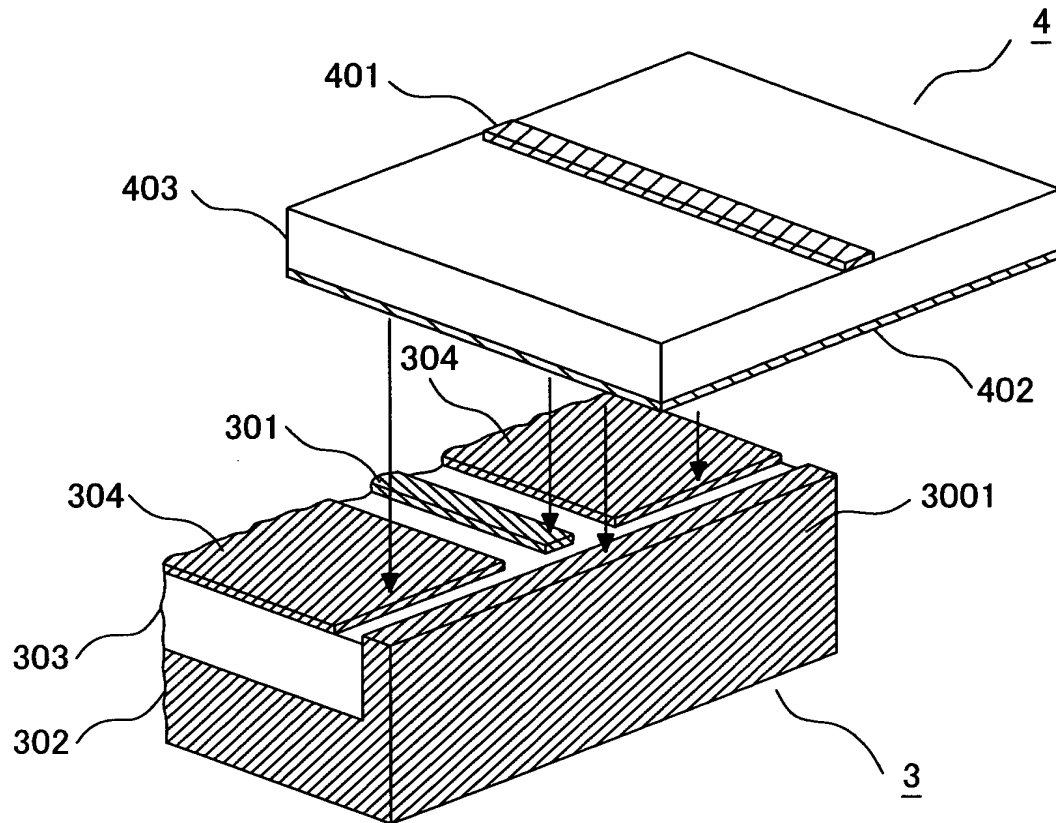


FIG.3B

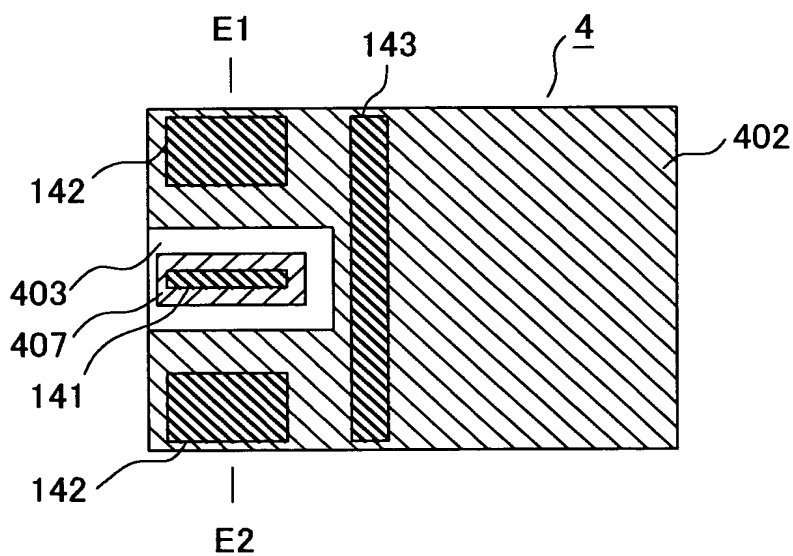
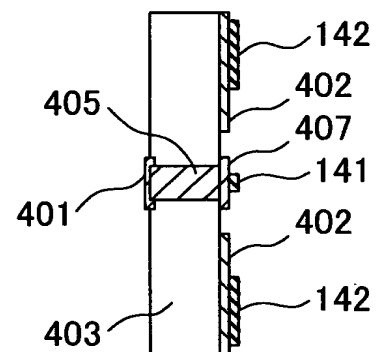


FIG.3C

E1-E2 SECTION



This diagram shows a cross-section of a semiconductor device with two main regions, 3 and 4. Region 3 (left) consists of layers 304, 301, F1, 303, G1, and another 304 layer. Region 4 (right) consists of layers 403, 401, F2, and G2. A central vertical section contains layers i1, H1 at the top and i2, H2 at the bottom, separated by a gap 3001.

F1-F2 SECTION

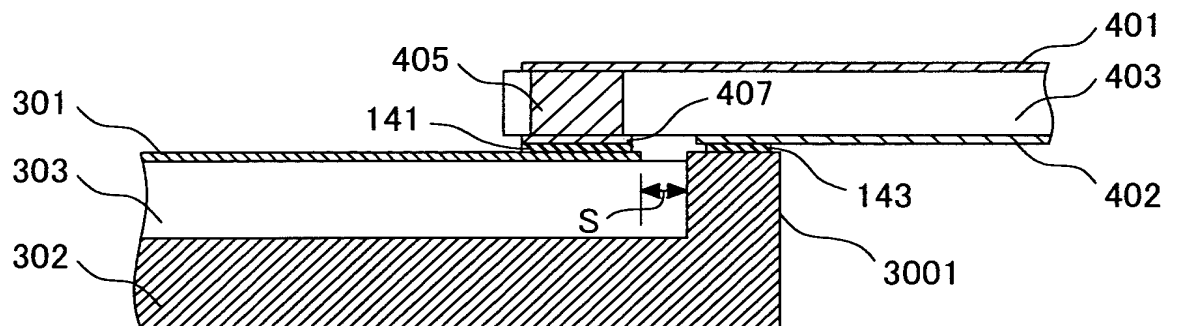


FIG.4C

G1-G2 SECTION

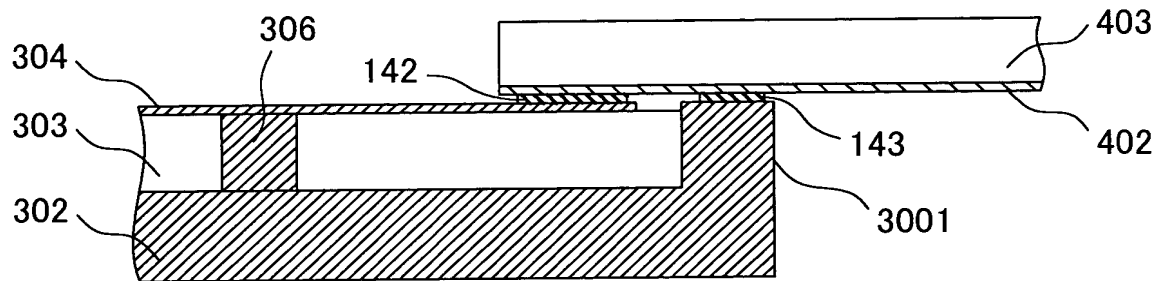


FIG.4D

H1-H2 SECTION

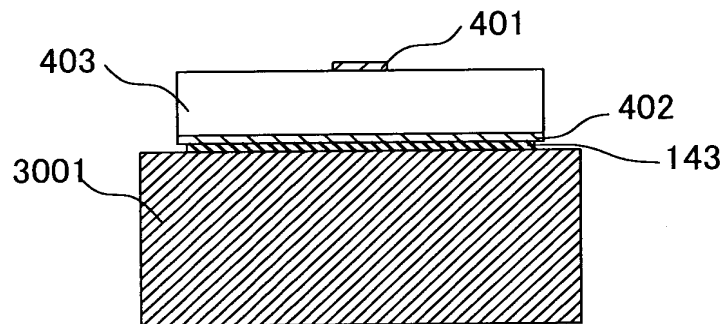


FIG.4E

i1-i2 SECTION

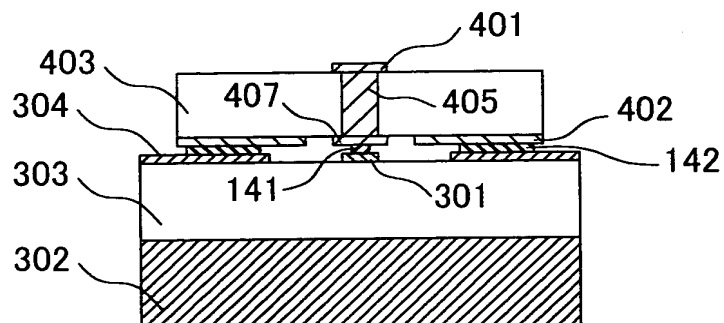


FIG.5A

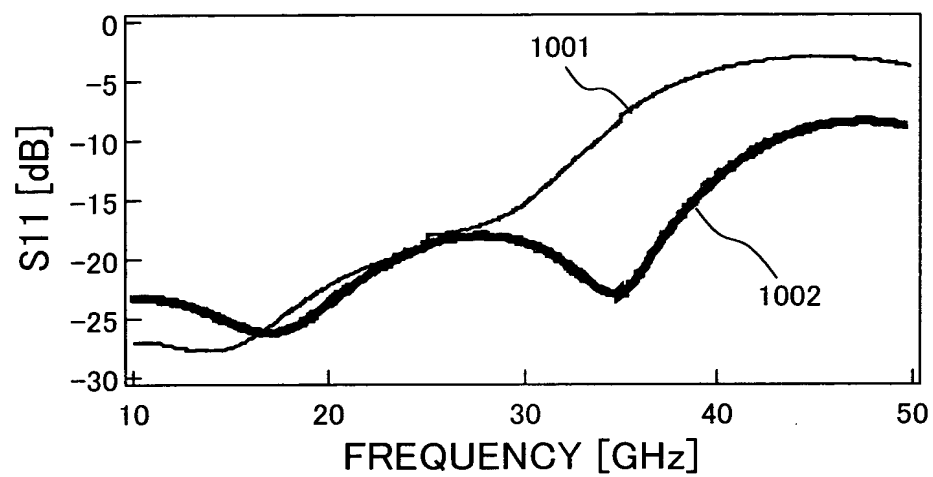


FIG.5B

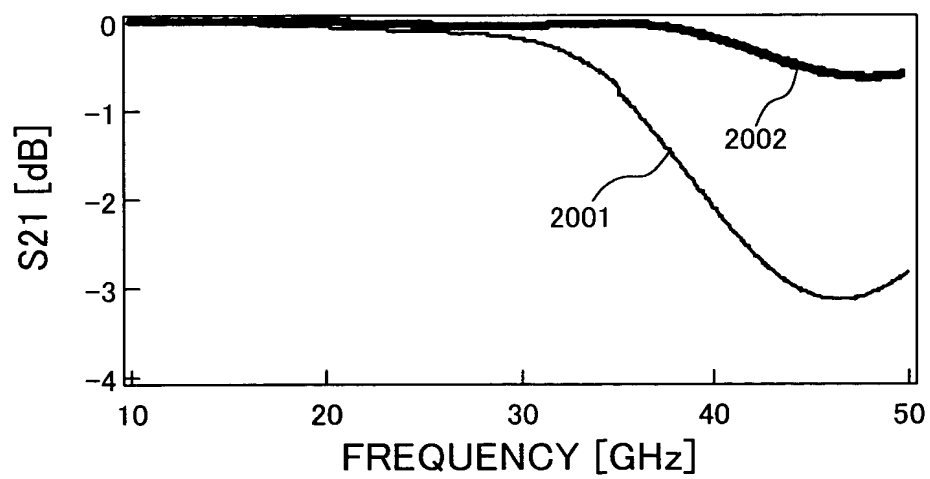


FIG.6A

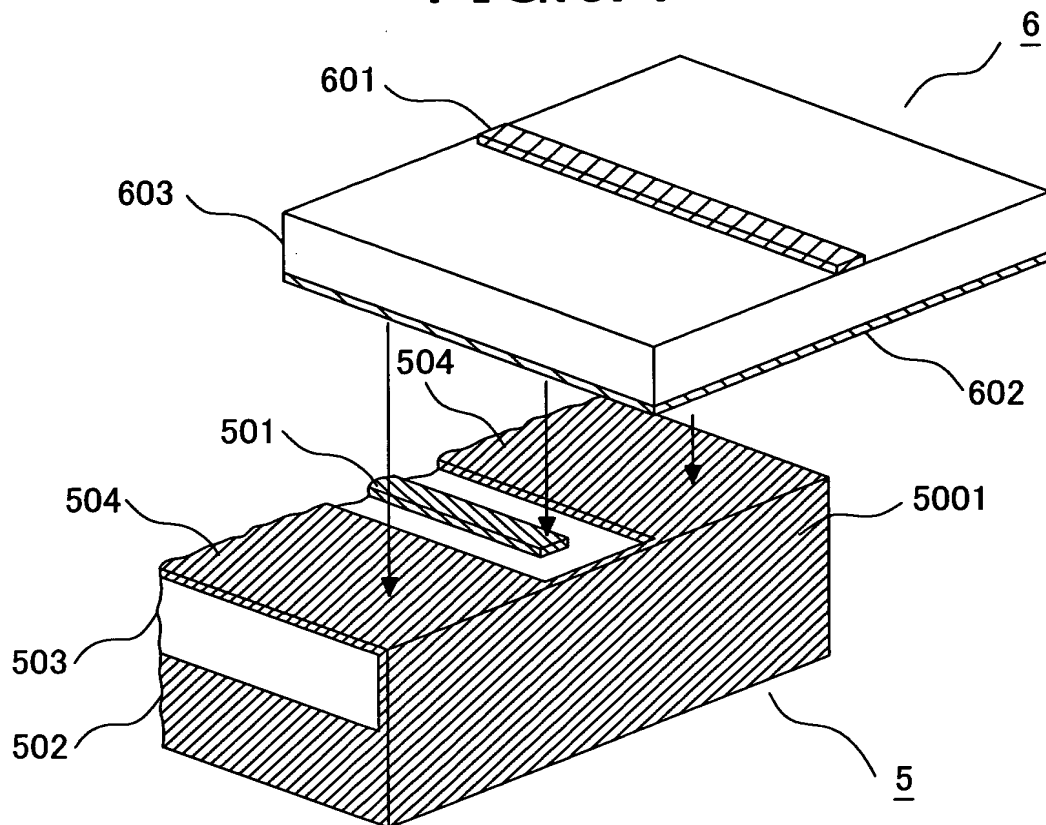


FIG.6B

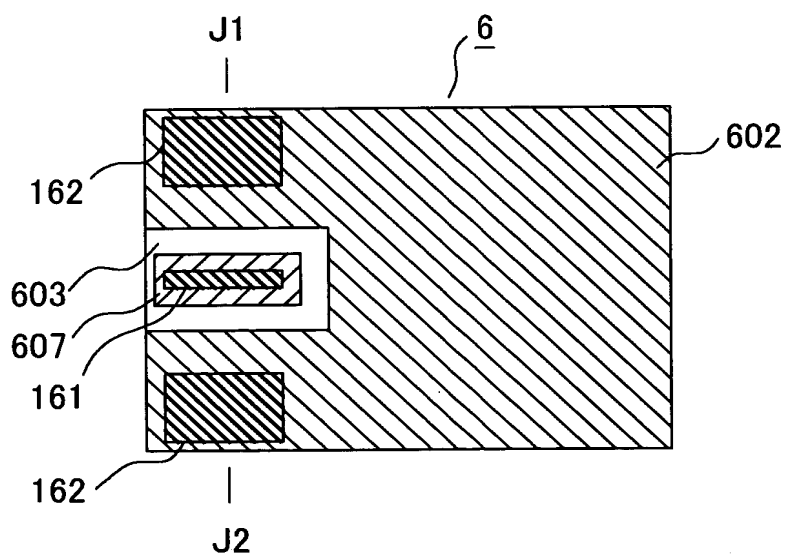


FIG.6C

J1-J2 SECTION

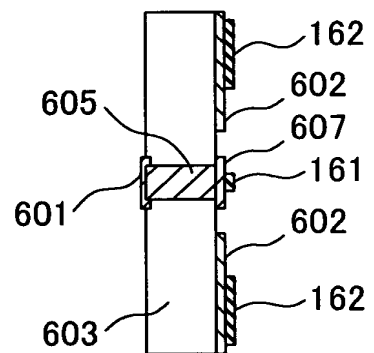


FIG.7A

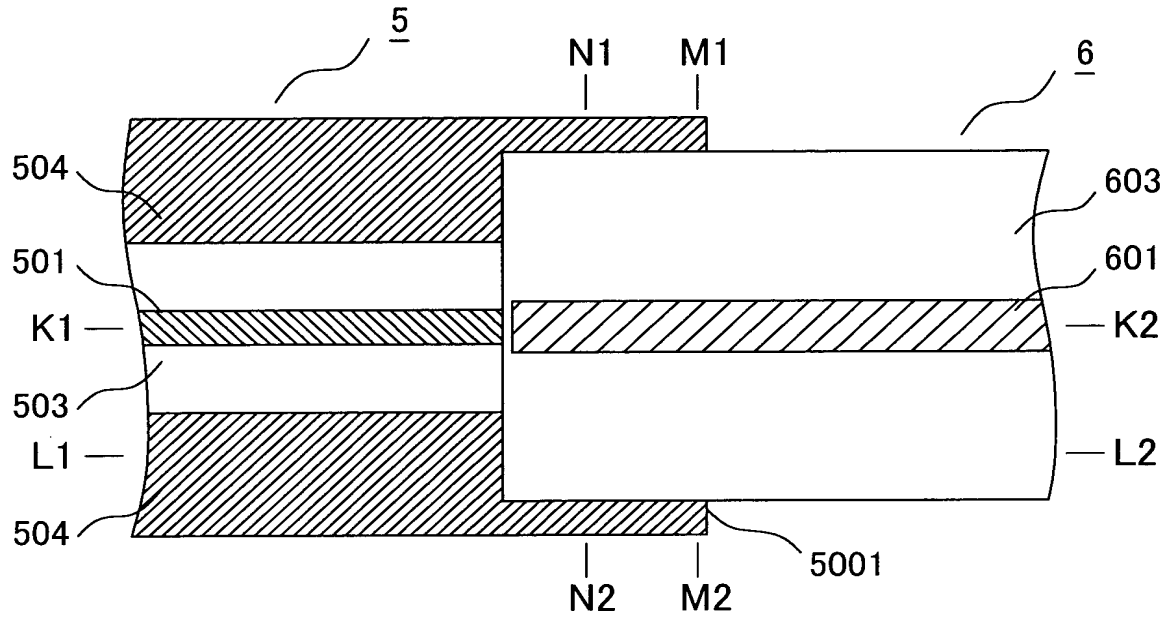


FIG.7B

K1-K2 SECTION

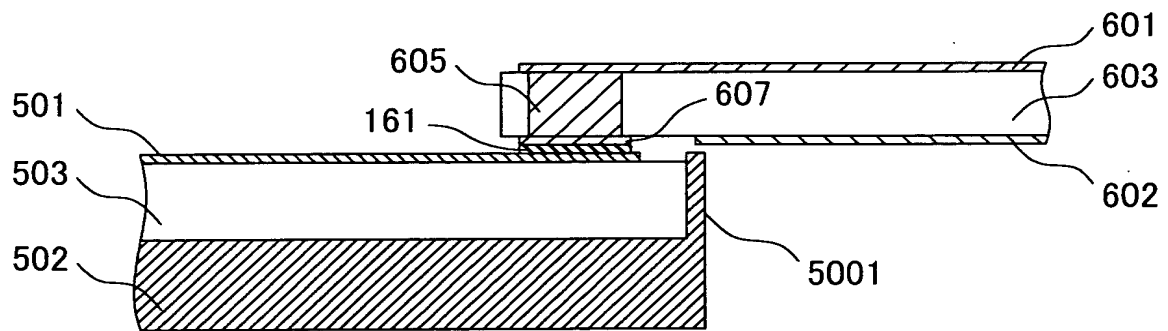


FIG.7C

L1-L2 SECTION

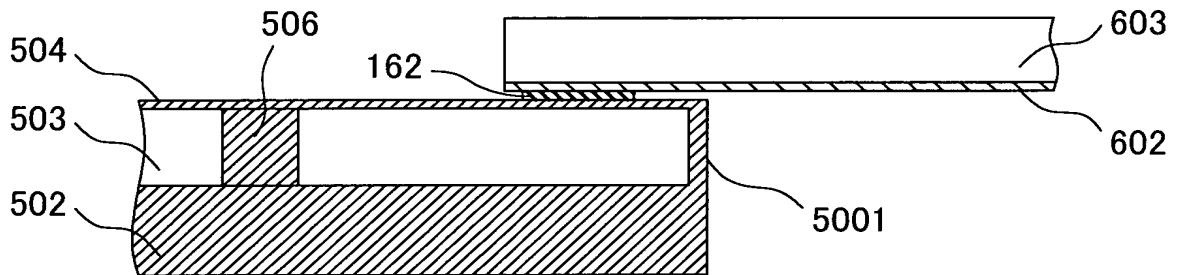


FIG.7D

M1-M2 SECTION

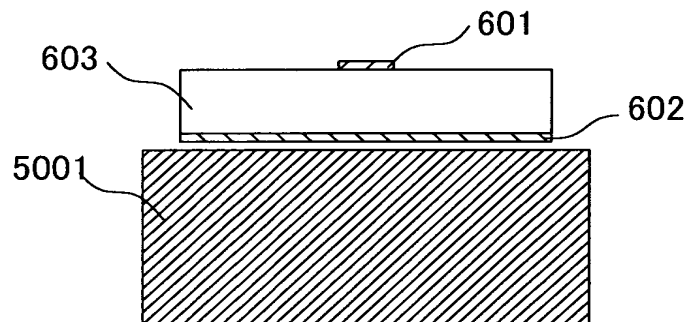


FIG.7E

N1-N2 SECTION

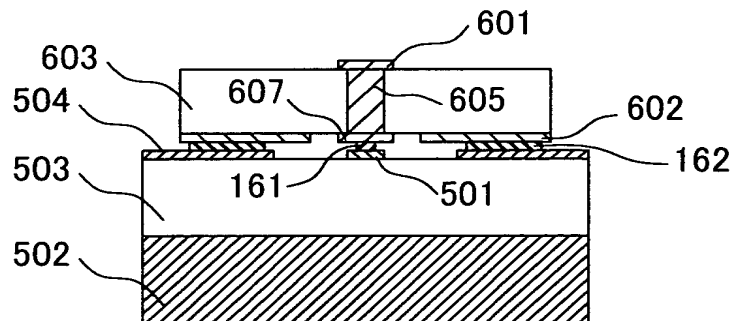


FIG.8A

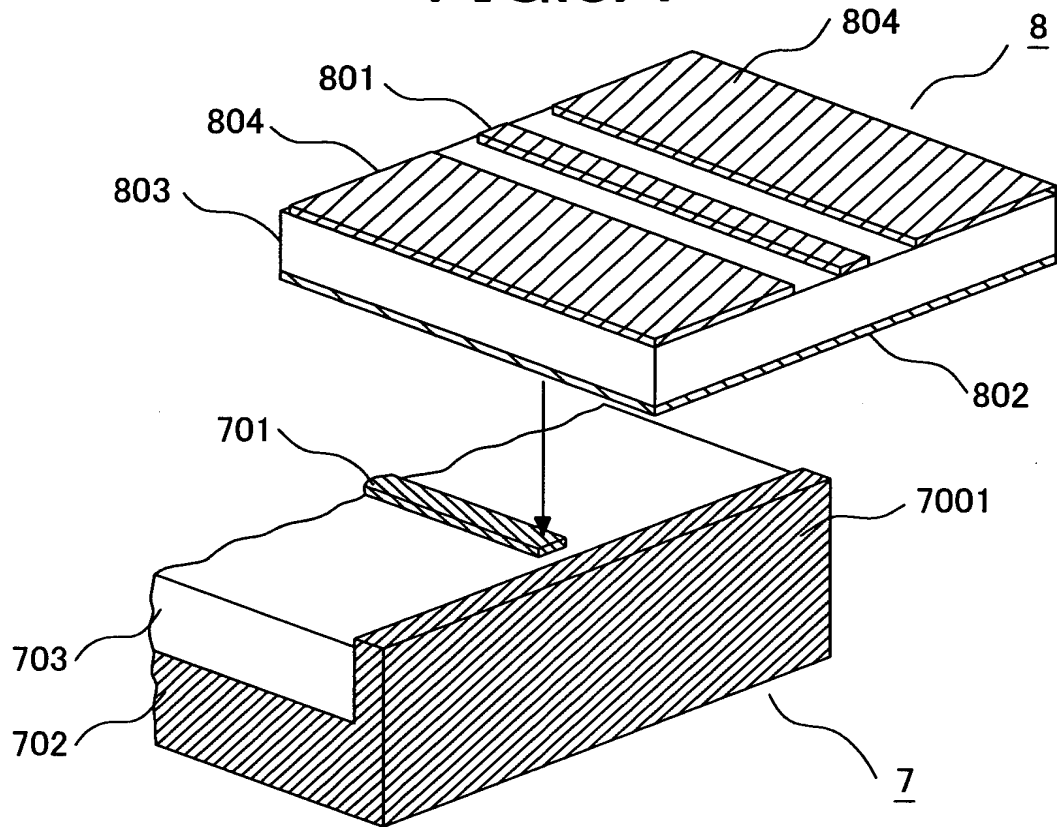


FIG.8B

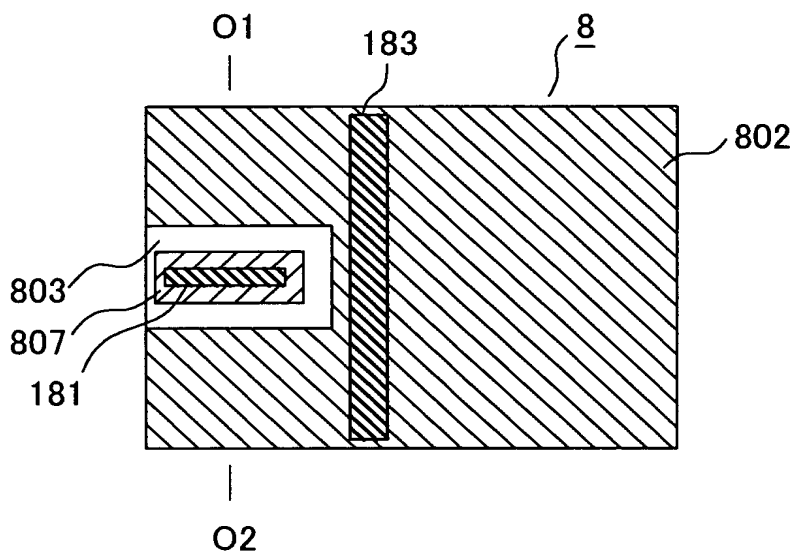


FIG.8C

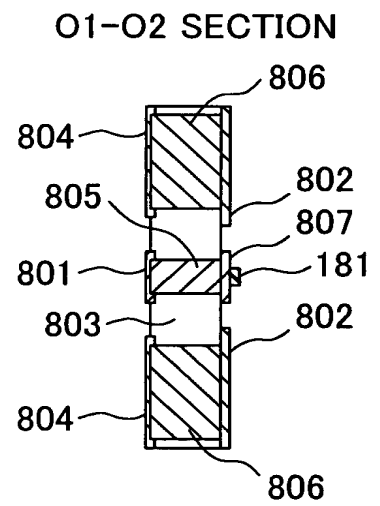


FIG.9A

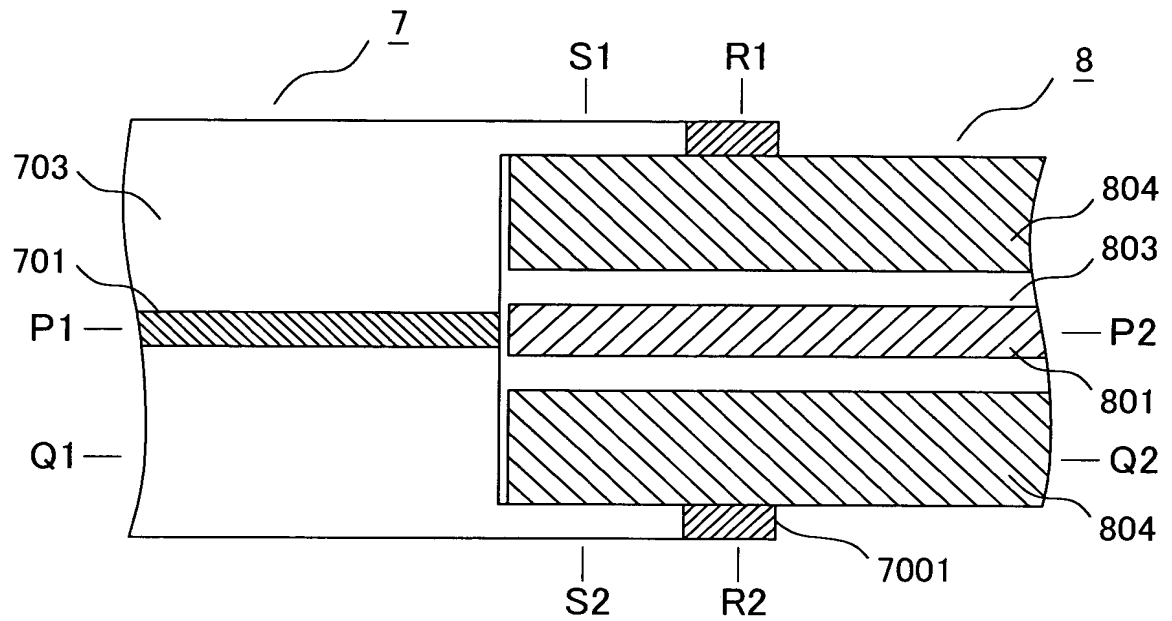


FIG.9B

P1-P2 SECTION

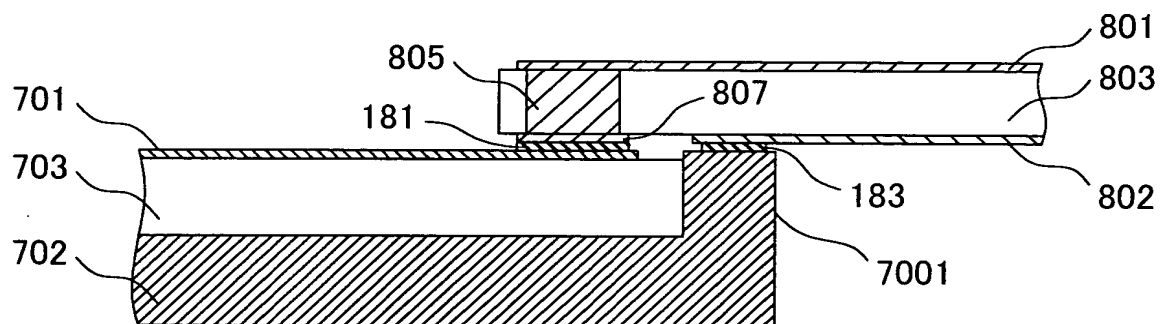


FIG.9C

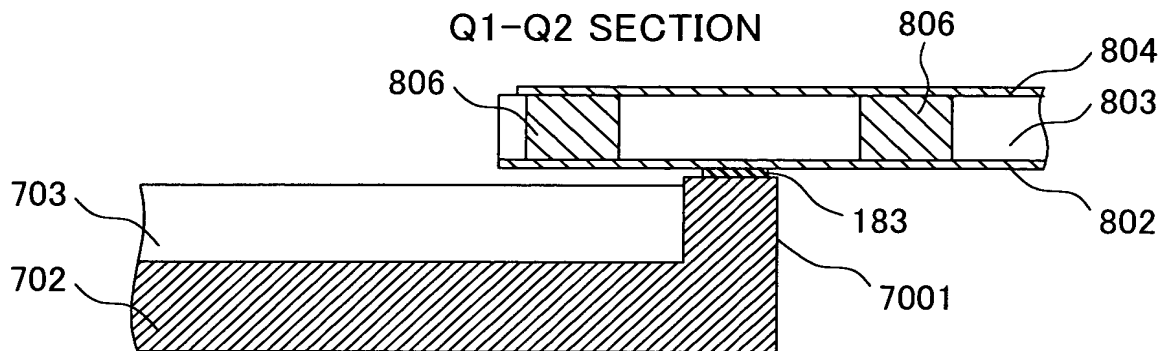


FIG.9D

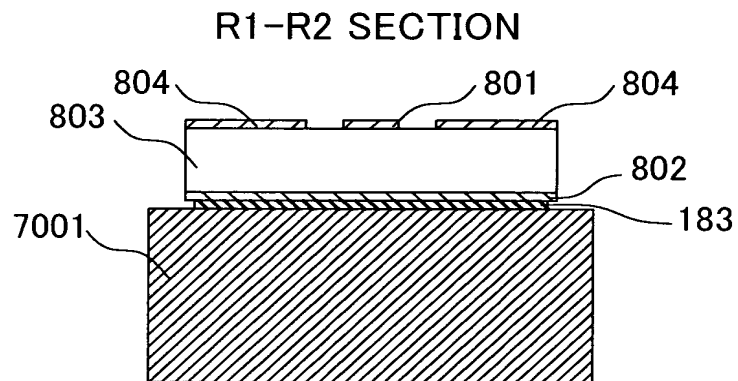


FIG.9E

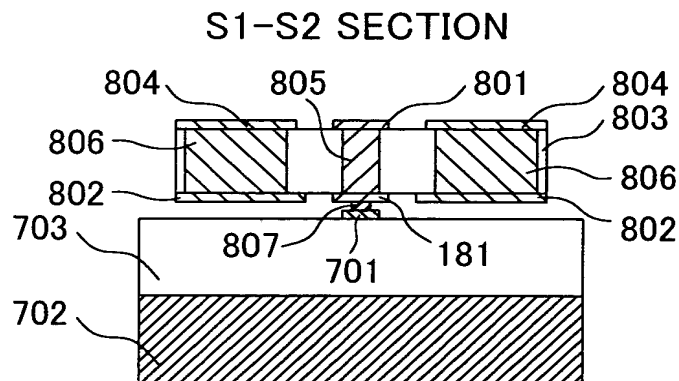


FIG.10

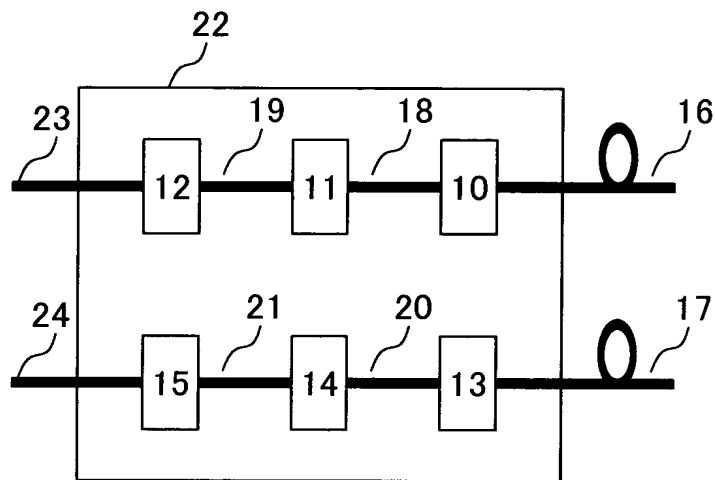


FIG.11

